



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: KOEMTZOPOULOS et al.

Attorney Docket No.:
LAM1P186/P1211

Application No.: 10/803,342

Examiner: PAGE, Thurman K.

Filed: March 17, 2004

Group: 1615

Title: DUAL DOPED POLYSILICON AND
SILICON GERMANIUM ETCH

Confirmation No.: 5586

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on November 17, 2005 in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signed: _____

Sue Funchess
Sue Funchess

**INFORMATION DISCLOSURE STATEMENT
37 CFR §§1.56 AND 1.97(b)**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

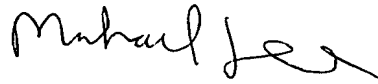
This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is: (i) filed within three (3) months of the filing date of the above-referenced application, (ii) believed to be filed before the mailing date of a first Office Action on the merits, or (iii) believed to be filed before the mailing of a first Office Action after the filing of a Request for Continued Examination under §1.114. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure

Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-0388 (Order No. LAM1P186).

Respectfully submitted,

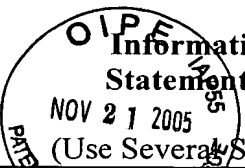
BEYER WEAVER & THOMAS, LLP

A handwritten signature in black ink, appearing to read "Michael Lee", with a stylized flourish at the end.

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Form 1449 (Modified)  Information Disclosure Statement By Applicant (Use Several Sheets if Necessary)	Atty Docket No.	Application No.:
	LAM1P186/P1211	10/803,342
Applicant:		
KOEMTZOPOULOS et al.		
Filing Date	Group	
March 17, 2004	1615	

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A1.	6,451,647B1	09/17/02	Yang et al.			03/18/02
	A2.	2003/0003752A1	01/02/03	Deshmukh et al.			06/27/01
	A3.	2003/0186492A1	10/02/03	Brown et al.			04/02/02
	A4.	2003/0227055A1	12/11/03	Bae et al.			01/13/03
	A5.	2004/0018739A1	01/29/04	Abooameri et al.			07/26/02
	A6.	2004/0033692A1	02/19/04	Yamazaki et al.			08/13/03

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	B1.	WO 98/13880	04/02/98	PCT			Yes	
	B2.	WO 00/04213	01/27/00	PCT			Yes	
	B3.	0 200 951	12/17/86	EPO			Yes	

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C1.	Kim, S. J. et al., "Notch- and foot-free dual polysilicon gate etch", Electrochemical Processing in ULSI Fabrication and Semiconductor/Metal Deposition II, Proceedings of the International Symposium (Electrochemical Society Proceedings Vol. 99-9), Electrochem. Soc., Pennington, NJ, USA, 1999, pages 361-365
	C2.	Vallon S. et al., "Poly-silicon-germanium gate patterning studies in a high density plasma helicon source", Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films), AIP for American Vacuum Soc. USA, vol. 15, no. 4, July 1997 (1997-07), pages 1874-1880
	C3.	Wang, C. S. et al., "Reactive ion etching of Si _{1-x} Ge _x alloy with hydrogen bromide", First International SiGe Technology and Device Meeting (ISTDM 2003) from Materials and Process Technology to Device and Circuit Technology, 15-17 Jan. 2003, Nagoya, Japan, vol. 224, no. 1-4, 15 March 2004, pages 222-226
	C4.	International Search Report, dated 10/25/05

Examiner	Date Considered
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Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.